1. A low power control circuit for transitioning a memory device between a first operating mode and a low power operating mode, said low power control circuit comprising:

a differential circuit connected to a reference voltage and a first control signal; and

a buffer circuit having an input connected to the first control signal;

wherein in the first operating mode said differential circuit is used to detect a first value of the first control signal and causes a transition from the first operating mode to the low power operating mode, and in the low power operating mode said buffer circuit and said differential circuit are used to detect a second value of the first control signal and cause a transition from the low power operating mode to the first operating mode.

2. The low power control circuit of claim 1, wherein the reference voltage is grounded during the low power operating mode.

3. The low power control circuit of claim 1, wherein the reference voltage is floated during the low power operating mode.

4. The low power control circuit of claim 1, wherein said differential circuit comprises a differential amplifier.

5. The low power control circuit of claim 1, wherein said buffer circuit comprises an inverter.

6. The low power control circuit of claim 1, further comprising a first logic circuit connected to the differential circuit and the buffer circuit, said first logic circuit disabling the buffer circuit and enabling the differential

circuit in the first operating mode, and in the low power mode, enabling the buffer circuit and disabling the differential circuit until the buffer circuit detects the second value.

7. The low power control circuit of claim 6, further comprising a second logic circuit coupled to the outputs of the buffer circuit and the differential circuit, said second logic circuit combining the outputs of the buffer circuit and the differential circuit to form an output causing the memory device to transition between the first and low power operating modes.

8. The low power control circuit of claim 6, wherein no current is applied to said differential circuit when disabled.

9. The low power control circuit of claim 6, wherein a reduced current is applied to said differential circuit when disabled.

10. The low power control circuit of claim 9, wherein a current reduced by about twenty-five percent of full current is applied to said differential circuit when disabled.

11. The low power control circuit of claim 9, wherein a current reduced by about seventy-five percent of full current is applied to said differential circuit when disabled.

12. The low power control circuit of claim 6, wherein said first logic circuit is connected to receive at least a second control signal indicative of a low power operation.

13. The low power control circuit of claim 12, wherein said low power operation is a self refresh operation.

14. The low power control circuit of claim 12, wherein said low power operation is a power down operation.

15. The low power control circuit of claim 1, wherein said first control signal is a clock enable signal.

16. The low power control circuit of claim 1, wherein said circuit is configured to perform low power control via an antifuse.

17. The low power control circuit of claim 1, wherein said circuit is configured to perform low power control via a metal mask.

18. The low power control circuit of claim 1, wherein said circuit is configured to ignore the reference voltage via an antifuse.

19. A low power control circuit for transitioning a memory device from a first operating mode to a low power operating mode when a first control signal has a first value, and transitioning the memory device from the low power operating mode to the first operating mode when the first control signal has a second value, said low power control circuit comprising:

a differential amplifier connected to a reference voltage and a first control signal;

a buffer circuit having an input connected to the first control signal; and

a first logic circuit connected to said differential amplifier and said buffer circuit, wherein in the first operating mode said first logic circuit disables the buffer circuit and enables the differential amplifier such that the differential amplifier is used to detect the first value, and in the low power

mode, enables the buffer circuit and disables the differential amplifier until the buffer circuit detects the second value,

wherein said memory device is transitioned to said first operating mode only after both said buffer circuit and said differential amplifier detect the second value.

20. The low power control circuit of claim 19, wherein the reference voltage is grounded during the low power operating mode.

21. The low power control circuit of claim 19, wherein the reference voltage is floated during the low power operating mode.

22. The low power control circuit of claim 19, further comprising a second logic circuit coupled to the outputs of the buffer circuit and the differential amplifier, said second logic circuit combining the outputs of the buffer circuit and the differential amplifier to form an output causing the memory device to transition between the first and low power operating modes.

23. The low power control circuit of claim 19, wherein said differential amplifier is completely choked when disabled.

24. The low power control circuit of claim 19, wherein said differential amplifier is partially choked when disabled.

25. The low power control circuit of claim 19, wherein said differential amplifier is mostly choked when disabled.

26. The low power control circuit of claim 19, wherein said first control signal is a clock enable signal.

27. A memory device comprising:

a low power control circuit for transitioning said memory device between a first operating mode and a low power operating mode, said low power control circuit comprising:

a differential circuit connected to a reference voltage and a first control signal; and

a buffer circuit having an input connected to the first control signal;

wherein in the first operating mode said differential circuit is used to detect a first value of the first control signal and causes a transition from the first operating mode to the low power operating mode, and in the low power operating mode said buffer circuit and said differential circuit are used to detect a second value of the first control signal and cause a transition from the low power operating mode to the first operating mode.

28. The memory device of claim 27, wherein the reference voltage is grounded during the low power operating mode.

29. The memory device of claim 27, wherein the reference voltage is floated during the low power operating mode.

30. The memory device of claim 27, wherein said low power control circuit further comprises a first logic circuit connected to the differential circuit and the buffer circuit, said first logic circuit disabling the buffer circuit and enabling the differential circuit in the first operating mode, and in the

low power mode, enabling the buffer circuit and disabling the differential circuit until the buffer circuit detects the second value.

31. The memory device of claim 30, wherein said low power control circuit further comprises a second logic circuit coupled to the outputs of the buffer circuit and the differential circuit, said second logic circuit combining the outputs of the buffer circuit and the differential circuit to form an output causing the memory device to transition between the first and low power operating modes.

32. The memory device of claim 30, wherein no current is applied to said differential circuit when disabled.

33. The memory device of claim 30, wherein a reduced current is applied to said differential circuit when disabled.

34. The memory device of claim 30, wherein a current reduced by about twenty-five percent of full current is applied to said differential circuit when disabled.

35. The memory device of claim 30, wherein a current reduced by about seventy-five percent of full current is applied to said differential circuit when disabled.

36. The memory device of claim 30, wherein said first logic circuit is connected to receive at least a second control signal indicative of a low power operation.

37. The memory device of claim 27, wherein said low power operation is a self refresh operation.

38. The memory device of claim 37, wherein said low power operation is a power down operation.

39. The memory device of claim 27, wherein said first control signal is a clock enable signal.

40. A memory device comprising:

a low power control circuit for transitioning said memory device from a first operating mode to a low power operating mode when a first control signal has a first value, and transitioning the memory device from the low power operating mode to the first operating mode when the first control signal has a second value, said low power control circuit comprising:

a differential amplifier connected to a reference voltage and a first control signal;

a buffer circuit having an input connected to the first control signal; and

a first logic circuit connected to said differential amplifier and said buffer circuit, wherein in the first operating mode said first logic circuit disables the buffer circuit and enables the differential amplifier such that the differential amplifier is used to detect the first value, and in the low power mode, enables the buffer circuit and disables the differential amplifier until the buffer circuit detects the second value,

wherein said memory device is transitioned to said first operating mode only after both said buffer circuit and said differential amplifier detect the second value.

41. The memory device of claim 40, wherein the reference voltage is grounded during the low power operating mode.

42. The memory device of claim 40, wherein the reference voltage is floated during the low power operating mode.

43. The memory device of claim 40, wherein said low power control circuit further comprises a second logic circuit coupled to the outputs of the buffer circuit and the differential amplifier, said second logic circuit combining the outputs of the buffer circuit and the differential amplifier to form an output causing the memory device to transition between the first and low power operating modes.

44. The memory device of claim 40, wherein said differential amplifier is completely choked when disabled.

45. The memory device of claim 40, wherein said differential amplifier is partially choked when disabled.

46. The memory device of claim 40, wherein said differential amplifier is mostly choked when disabled.

47. The memory device of claim 40, wherein said first control signal is a clock enable signal.

48. A processor system comprising:

a processor; and

a memory device comprising a low power control circuit for transitioning said memory device between a first operating mode and a low power operating mode, said low power control circuit comprising:

a differential circuit connected to a reference voltage and a first control signal, and

a buffer circuit having an input connected to the first control signal,

wherein in the first operating mode said differential circuit is used to detect a first value of the first control signal and causes a transition from the first operating mode to the low power operating mode, and in the low power operating mode said buffer circuit and said differential circuit are used to detect a second value of the first control signal and cause a transition from the low power operating mode to the first operating mode.

49. The system of claim 48, wherein the reference voltage is grounded during the low power operating mode.

50. The system of claim 48, wherein the reference voltage is floated during the low power operating mode.

51. The system of claim 48, wherein said low power control circuit further comprises a first logic circuit connected to the differential circuit and the buffer circuit, said first logic circuit disabling the buffer circuit and enabling the differential circuit in the first operating mode, and in the low power mode, enabling the buffer circuit and disabling the differential circuit until the buffer circuit detects the second value.

52. The system of claim 48, wherein no current is applied to said differential circuit when disabled.

53. The system of claim 48, wherein a reduced current is applied to said differential circuit when disabled.

54. The system of claim 48, wherein a current reduced by about twenty-five percent of full current is applied to said differential circuit when disabled.

55. The system of claim 48, wherein a current reduced by about seventy-five percent of full current is applied to said differential circuit when disabled.

56. The system of claim 48, wherein said first logic circuit is connected to receive at least a second control signal indicative of a low power operation.

57. A processor system comprising:

a processor; and

a memory device including a low power control circuit for transitioning said memory device from a first operating mode to a low power operating mode when a first control signal has a first value, and transitioning the memory device from the low power operating mode to the first operating mode when the first control signal has a second value, said low power control circuit comprising:

a differential amplifier connected to a reference voltage and a first control signal,

a buffer circuit having an input connected to the first control signal, and

a first logic circuit connected to said differential amplifier and said buffer circuit, wherein in the first operating mode said first logic circuit disables the buffer circuit and enables the differential amplifier such that the differential amplifier is used to detect the first value, and in the low power mode, enables the buffer circuit and disables the differential amplifier until the buffer circuit detects the second value,

wherein said memory device is transitioned to said first operating mode only after both said buffer circuit and said differential amplifier detect the second value.

58. The system of claim 57, wherein the reference voltage is grounded during the low power operating mode.

59. The system of claim 57, wherein the reference voltage is floated during the low power operating mode.

60. The system of claim 57, wherein said low power control circuit further comprises a second logic circuit coupled to the outputs of the buffer circuit and the differential amplifier, said second logic circuit combining the outputs of the buffer circuit and the differential amplifier to form an output causing the memory device to transition between the first and low power operating modes.

61. The system of claim 57, wherein said differential amplifier is completely choked when disabled.

62. The system of claim 57, wherein said differential amplifier is partially choked when disabled.

63. The system of claim 57, wherein said differential amplifier is mostly choked when disabled.

64. The system of claim 57, wherein said first control signal is a clock enable signal.

65. A method of transitioning a memory device between a first operating mode and a low power operating mode, said method comprising:

detecting, using a differential circuit, when a first control signal has a first value;

transitioning the memory device from the first operating mode to the low power operating mode;

disabling the differential circuit;

enabling a buffer circuit;

detecting, at the buffer circuit, when the first control signal has a second value;

enabling the differential circuit;

detecting, at the buffer circuit and the differential circuit, when the first control signal has the second value; and

transitioning the memory device from the low power operating mode to the first operating mode.

66. The method of claim 65, wherein said step of disabling the differential circuit comprises completely choking the differential circuit.

67. The method of claim 65, wherein said step of disabling the differential circuit comprises partially choking the differential circuit.

68. The method of claim 65, wherein said step of disabling the differential circuit comprises mostly choking the differential circuit.

69. The method of claim 65 further comprising the step of grounding a reference voltage connected to the differential circuit during the low power operating mode.

70. The method of claim 65 further comprising the step of floating a reference voltage connected to the differential circuit during the low power operating mode.

71. A method of transitioning a memory device between a first operating mode and a low power operating mode, said method comprising:

comparing a first control signal to a reference voltage;

determining whether the first control signal has a first value based on the comparison;

transitioning the memory device from the first operating mode to the low power operating mode if the first control signal has the first value;

determining when the first control signal has a second value;

ensuring that the first control signal has the second value; and

transitioning the memory device from the low power operating mode to the first operating mode if it is ensured that the first control signal has the second value.

72. The method of claim 71 further comprising the step of grounding the reference voltage during the low power operating mode.

73. The method of claim 71 further comprising the step of floating the reference voltage during the low power operating mode.

74. The method of claim 71, wherein said ensuring step comprises comparing the first control signal to the reference voltage once it is determined that the first control signal has the first value.

75. The method of claim 71 further comprising the step of programming an antifuse.

76. The method of claim 71 further comprising the step of setting a switch in a metal mask.